WHAT IS CLAIMED IS:

1. An integrated circuit device, the device comprising:

a substrate;

an insulating layer overlying the substrate;

a copper metal layer overlying the insulating layer;

an etch stop layer overlying the copper metal layer;

an interlayer dielectric material overlying the etch stop layer, the interlayer dielectric material including an upper surface;

a plurality of via openings defined within a region of the interlayer dielectric layer from the upper surface through the etch stop layer to the copper metal layer;

a copper fill material within each of the plurality of via openings to define a plurality of copper structure extending from the upper surface through the etch stop layer to the copper metal layer;

a first barrier metal layer overlying each of the plurality of copper structures to define a first electrode of a capacitor structure;

an insulating layer overlying the first barrier metal layer to define an insulating layer for the capacitor structure; and

a second barrier metal layer overlying the insulating layer to define the second electrode.

2. The device claim 1 wherein the insulating layer is silicon nitride and the etch stop layer is nitride.

3. The device of claim 1 wherein the insulating layer has a thickness of about 200 to about 1000 Angstroms and more preferably 300 to 700 Angstroms.

4. The device of claim 1 wherein the insulating layer is PECVD nitride.

5. The device of claim 1 wherein the first barrier metal layer and the second barrier metal layer comprises a tantalum material or a titanium material.

6. The device of claim 1 wherein each of the plurality of metal structures has a width of less than 0.3 microns and a height of greater than about 7000 Angstroms.

7. The device of claim 1 wherein the capacitor structure has a capacitance ranging from about 0.5 to about 5 Fempto Farads per square micron.

8. The device of claim 1 further comprising a metal connector layer overlying the second barrier metal layer.

9. The device of claim 1 wherein the plurality of metal structures includes at least ten or more.

10. The device of claim 1 wherein the copper layer comprises a second portion, the second portion defines an interconnect layer.

11. An integrated circuit device, the device comprising:

a substrate;

an insulating layer overlying the substrate;

a copper metal interconnect layer overlying the insulating layer;

a capping layer overlying the copper interconnect metal layer to isolate the copper metal interconnect layer form overlying structures;

a first barrier metal layer overlying the capping layer, the first barrier metal layer being free from the copper interconnect layer to define a first electrode structure;

an insulating layer overlying the first barrier metal layer to define a capacitor dielectric structure;

a second barrier metal layer overlying the insulating layer to define a second electrode structure;

an etch stop layer overlying the second barrier metal layer;

an interlayer dielectric material overlying the etch stop layer, the interlayer dielectric material including an upper surface;

a plurality of via openings defined within a region of the interlayer dielectric layer from the upper surface through the etch stop layer to the second barrier metal layer;

a copper fill material within each of the plurality of via openings to define a plurality of copper structure extending from the upper surface through the etch stop layer to the second barrier metal layer; and

an upper metal layer formed overlying the plurality of copper metal structures.

12. The device of claim 11 wherein the capping layer and the first barrier metal layer maintain the capacitor insulating layer free from copper impurities.

13. The device of claim 11 wherein the capping layer maintains the capacitor-insulating layer free from copper impurities during subsequent processing of the device.

14. The device of claim 11 wherein the device is a mixed signal device having a frequency range from about 1 MHz and greater.

15. The device of claim 11 wherein the capping layer PE CVD nitride.

16. The device of claim 11 wherein the capping layer has a thickness of over 300 Angstroms.

17. A method for manufacturing integrated circuit devices, the method comprising:

providing a substrate;

forming an insulating layer overlying the substrate;

forming a copper metal interconnect layer overlying the insulating layer;

forming a capping layer overlying the copper interconnect metal layer to isolate the copper metal interconnect layer form overlying structures;

forming a first barrier metal layer overlying the capping layer, the first barrier metal layer being free from the copper interconnect layer to define a first electrode structure;

forming an insulating layer overlying the first barrier metal layer to define a capacitor dielectric structure;

forming a second barrier metal layer overlying the insulating layer to define a second electrode structure;

forming an etch stop layer overlying the second barrier metal layer;

forming an interlayer dielectric material overlying the etch stop layer, the interlayer dielectric material including an upper surface;

forming a plurality of via openings defined within a region of the interlayer dielectric layer from the upper surface through the etch stop layer to the second barrier metal layer;

providing a copper fill material within each of the plurality of via openings to define a plurality of copper structure extending from the upper surface through the etch stop layer to the second barrier metal layer; and

forming an upper metal layer formed overlying the plurality of copper metal structures.

18. The method of claim 17 further comprising planarizing exposed portions of the copper fill material.

19. The method of claim 17 wherein the upper metal layer comprises copper material.

20. A method for forming an integrated circuit device, the method comprising:

providing a substrate;

forming an insulating layer overlying the substrate;

forming a copper metal layer overlying the insulating layer;

forming an etch stop layer overlying the copper metal layer;

forming an interlayer dielectric material overlying the etch stop layer, the interlayer dielectric material including an upper surface;

forming a plurality of via openings defined within a region of the interlayer dielectric layer from the upper surface through the etch stop layer to the copper metal layer;

forming a copper fill material within each of the plurality of via openings to define a plurality of copper structure extending from the upper surface through the etch stop layer to the copper metal layer;

forming a first barrier metal layer overlying each of the plurality of copper structures to define a first electrode of a capacitor structure;

forming an insulating layer overlying the first barrier metal layer to define an insulating layer for the capacitor structure; and

forming a second barrier metal layer overlying the insulating layer to define the second electrode.